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APPLICANT:	Toshimasa Kobayashi, et al.	ATTY. DOCKET NO.	09794353-0033
SERIAL NO.	10/813,528	GROUP ART UNIT:	2812
DATE FILED:	March 30, 2004	EXAMINER:	S. Mulpuri
INVENTION:	"METHOD OF MANUFACTURING A SEMICONDUCTOR LIGHT EMITTING DEVICE, SEMICONDUCTOR LIGHT EMITTING DEVICE, METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE, SEMICONDUCTOR DEVICE, METHOD OF MANUFACTURING A DEVICE, AND DEVICE"		

Affidavit Under 37 CFR §1.131

S I R:

We, Toshimasa Kobayashi and Kensaku Motoki (herein after 'We' or 'Affiant'), hereby declare as follows:

1. We are the joint inventors of Method of Manufacturing a Semiconductor Light Emitting Device, Semiconductor Light Emitting Device, Method of Manufacturing a Semiconductor Device, Semiconductor Device, Method of Manufacturing a Device, and Device, which is the subject matter of the application for United States Patent Application No. 10/813,528 (" '528 application"), filed 30 March 2004.

2. In the Office Action mailed on 08 March 2007, the Examiner cites U.S. Publication No. 2005/0076830 by *Motoki, et al. ("Motoki '830")* as grounds for obviousness to reject claims 1-8, 12-18, 20, 21, 27-39, 42, 44, 46, 48, 50, 52, 54, and 56 of the '528 application.

3. *Motoki '830* has a U.S. filing date of 09 September 2004 and is a continuation-in-part of U.S. Serial No. 10/265,719 ("*Motoki '719*"), which was filed on 08 October 2002.

4. This is a declaration of prior invention to overcome *Motoki '830*. As inventors of the subject matter of the rejected claims, we hereby submit this Affidavit to overcome *Motoki '830*.

5. Exhibit A is a copy of Japanese Application No. 2001-315705 ("JP '705 application"), which was filed in Japan on 12 October 2001, prior to *Motoki '719's* (*Motoki '830's* parent application) U.S. filing date of 08 October 2002. A certified translation of the JP '705 application is also submitted herewith as Exhibit B.

6. We are the only named inventors of the '528 application and the JP '705 application.

7. The JP '705 application discloses conception of the subject matter of at least claims 1-8, 12-18, 20, 21, 27-39, 42, 44, 46, 48, 50, 52, 54, and 56 of the '528 application at least as early as 12 October 2001. Specifically, the JP '705 application discloses a method of producing a device having a structured substrate including stripe-shaped second regions that are arranged in parallel in a first region made of crystal. (*See, e.g.,* Figure 25 of certified translation of JP '705

application, illustrative stripe-shaped second regions B arranged in parallel in first region A). The second regions have an average dislocation density that is greater than the average dislocation density of the first region. (*See, e.g.,* Figure 3 of certified translation of JP '705 application, dislocation density decreases with distance from center of second region B; Paragraph [0186] of certified translation of JP '705 application, average dislocation density of second regions B is greater than average dislocation density of first region A).

8. The JP '705 application was filed on 12 October 2001 and published in Japan on 25 April 2003 as publication number JP 2003-124115. Less than one year after the publication in Japan of the JP '705 application, the '528 application was filed in the U.S. on 30 March 2004.

9. We allege that the acts relied upon to establish an invention date prior to the filing date of *Motoki '830* were carried out in Japan.

10. We hereby declare that the statements made of our own knowledge are true and that all statements made on information and belief are believed to be true. We acknowledge that willful false statements and the like are punishable by fine or imprisonment, or both (18 U.S.C. 1001) and may jeopardize the validity of the application or any patent issuing thereon.

Toshimasa Kobayashi

Toshimasa Kobayashi Date: Sep 21 2007

Kensaku Motoki

_____ Date: _____